Claims

[c1] A method of forming an FinFET device, comprising:
(a) providing a semiconductor substrate,
(b) forming a dielectric layer on a top surface of said substrate;
(c) forming a silicon fin on a top surface of said dielectric layer;
(d) forming a protective layer on at least one sidewall of said fin; and
(e) removing said protective layer from said at least one sidewall in a channel region of said fin.

[c2] The method of claim 1, further including between steps (d) and (e) performing at least one ion implantation step into said fin.

[c3] The method of claim 1, further including:
(f) forming a gate dielectric on exposed surfaces of said fin in said channel region; and
(g) forming a conductive gate on said gate dielectric.

[c4] The method of claim 3, further including:
(h) removing said protective layer from source/drain regions of said fin.

[c5] The method of claim 1, further including between steps (c) and (d) removing a portion of said dielectric layer from under said fin.

[c6] The method of claim 1, wherein said protective layer comprises tetraethoxysilane oxide or silicon nitride.

[c7] The method of claim 1, wherein said protective layer is about 15 to 50 Å thick.

[c8] The method of claim 1, wherein said fin has a height of about 500 to 2000 Å and has a width of about 200 to 500 Å.

[c9] The method of claim 1, wherein step (c) comprises:
forming a silicon layer on said top surface of said dielectric layer;
forming a mask over said silicon layer;
removing portions of said silicon layer not protected by said mask to expose said dielectric layer; and
removing said mask.

[c10] The method of claim 1, wherein said fin comprises mono-crystalline silicon.

[c11] A method of forming an FinFET device, comprising:
(a) providing a semiconductor substrate,
(b) forming a dielectric layer on a top surface of said

substrate;
(c) forming a silicon fin having sidewalls on a top surface of said dielectric layer; and
(d) forming a protective spacer on at least a lower portion of at least one of said sidewalls.

[c12] The method of claim 11, further including:
(e) performing at least one ion implantation step into said fin.

[c13] The method of claim 11, further including:
(e) forming a gate dielectric on exposed surfaces of said fin in at least a channel region of said fin; and
(f) forming a conductive gate on said gate dielectric.

[c14] The method of claim 11, further including between steps (c) and (d) removing a portion of said dielectric layer from under said fin.

[c15] The method of claim 11, wherein said protective spacer comprises tetraethoxysilane oxide or silicon nitride.

[c16] The method of claim 11, wherein said protective spacer is about 15 to 50 Å thick.

[c17] The method of claim 11, wherein said fin has a height of about 500 to 2000 Å and has a width of about 200 to 500 Å.

[c18] The method of claim 11, wherein step (c) comprises:
forming a silicon layer on said top surface of said mask over said silicon layer;
removing portions of said silicon layer not protected by said mask to expose said dielectric layer; and
removing said mask.

[c19] The method of claim 11, wherein step (c) comprises:
forming a mandrel on said dielectric layer;
depositing a conformal silicon layer on a top surface and a sidewall of said mandrel and on surfaces of said dielectric layer not covered by said mandrel;
removing said conformal silicon layer from said top surface of said mandrel and said surfaces of said dielectric layer not covered by said mandrel.

[c20] The method of claim 19, further including after the step of removing, performing a high temperature anneal of said conformal silicon layer.

[c21] The method of claim 11, wherein said fin comprises mono-crystalline silicon.

[c22] An FinFET device, comprising:
a semiconductor substrate,
a dielectric layer on a top surface of said substrate;
a silicon fin having sidewalls, said fin on a top surface of

said dielectric layer; and
a protective spacer on at least a lower portion of at least one of said sidewalls.

[c23] The FinFET device of claim 22, wherein said fin includes a channel region and source/drain regions.

[c24] The FinFET device of claim 22, further including:
a gate dielectric on surfaces of said fin in said channel region of said fin; and
a conductive gate on said gate dielectric.

[c25] The FinFET device of claim 22, wherein said protective spacer comprises tetraethoxysilane oxide or silicon nitride.

[c26] The FinFET device of claim 22, wherein said protective spacer is about 15 to 50 Å thick.

[c27] The FinFET device of claim 22, wherein said fin has a height of about 500 to 2000 Å and has a width of about 200 to 500 Å.

[c28] The FinFET device of claim 22, wherein said silicon fin comprises mono-crystalline silicon.